*509 F.2d 566, *; 1975 CCPA LEXIS 185, **;*
184 U.S.P.Q. (BNA) 607

IN THE MATTER OF THE APPLICATION OF KOSEI NOMIYA, TOSHIHIKO KOHISA AND ISAO MATSUMURA

Patent Appeal No. 74-514

UNITED STATES COURT OF CUSTOMS AND PATENT APPEALS

509 F.2d 566; 1975 CCPA LEXIS 185; 184 U.S.P.Q. (BNA) 607

February 6, 1975

PRIOR HISTORY: [1]**

Serial No. 768,794.

CASE SUMMARY

PROCEDURAL POSTURE: Appellants sought review of the Patent Office Board of Appeals rejection, under 35 U.S.C.S. § 103, of their patent claims for semiconductor circuit devices using insulated gate-type field effect elements having protective diodes.

OVERVIEW: Appellants sought to patent their claims for semiconductor circuit devices using insulated gate-type field effect elements having protective diodes. Appellants' application contained figures that were labeled prior art. The Patent Office Board of Appeals rejected their claims under 35 U.S.C.S. § 103. Appellants argued that the figures labeled prior art did show the prior art, but they also showed appellants' improvements to the prior art because of their solution to a problem that was not known by the prior art. The court reversed the board's rejection of appellants' claims. The court reasoned that the prior art structures in the figures did not suggest the problem that the appellants discovered and corrected through their patent claims. There was no evidentiary basis for the finding that a person of ordinary skill in the art would have had reason to apply an additional shunt diode to the prior art already equipped with a protective diode formed in the same substrate.

OUTCOME: Board's rejection of appellants' patent claims for obviousness due to a prior art was reversed because appellants expected and solved a problem with the prior art that a person of ordinary skill in the art at the time of invention would not have expected to exist.

CORE TERMS: diode, substrate, region, junction, drain, signal, transistor, protective, invention, biased, semiconductor, gate, input, voltage, teaching, bipolar, noise, connected, parasitic, skill, insulated, carrier, bias, insulating, examiner, field-effect, memory, shunt, obviousness, electrode

LexisNexis (TM) HEADNOTES - Core Concepts - ◆ Hide Concepts

Patent Law > Novelty & Anticipation

HN1 A statement by an applicant, whether in the application or in other papers submitted during prosecution, that certain matter is "prior art" to him, is an admission that that matter is prior art for all purposes, whether or not a basis in 35 U.S.C.S. § 102 can be found for its use as prior art. More Like This Headnote

Patent Law > Nonobviousness > Tests & Proof of Obviousness

HN2 A patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the "subject

matter as a whole" which should always be considered in determining the obviousness of an invention under 35 U.S.C.S. § 103. More Like This Headnote

Patent Law > Nonobviousness > Tests & Proof of Obviousness

HN3 If there is no evidence of record that a person of ordinary skill in the art at the time of invention would have expected the problem to exist at all, it is not proper to conclude that the invention which solves this problem, which is claimed as an improvement of the prior art device, would have been obvious to that hypothetical person of ordinary skill in the art. More Like This Headnote

OPINIONBY: RICH

OPINION: [*566]

RICH, Judge.

This appeal is from the decision of the Patent Office n1 Board of Appeals affirming the rejection under 35 USC 103 of claims 1-8 and 33 in application serial No. 768,794, filed October 18, 1968, for "Semiconductor Circuit Devices Using Insulated Gate-Type Field Effect Elements Having Protective Diodes." We reverse.

n1 Pub. L. 93-596, effective January 2, 1975, changed the names of the Patent Office and the Commissioner of Patents to the "Patent and Trademark Office" and the "Commissioner of Patents and Trademarks," respectively. For convenience and brevity hereinafter we shall use the abbreviation PTO.

The Invention

Appellants' invention pertains to insulated-gate-type field-effect transistors (hereinafter IGFET) and their use in **[*567]** semiconductor capacitive memory circuits having very low capacitance. For ease of discussion we reproduce Figs. 1 and 2 of the application:

[Graphic omitted. See illustration in original.]

The structure of Q(1) in Fig. 1 is an IGFET, consisting of two P-type n2 regions, S(1) and D(1), diffused into an N-type starting crystal, or substrate, usually of silicon, **[**2]** with an insulating oxide layer SiO(2) formed on the surface of the N-type substrate and contacting the diffused P-type regions. A metal gate electrode G(1) is attached to the insulating layer. IGFETs used as switching devices, as contemplated by appellants, are customarily fabricated in the OFF-mode. In this mode, when no voltage is applied to the gate, the two P-type regions, called source (S(1)) and drain (D(1)), are electrically insulated from each other by the N-type region surrounding them. However, when a negative voltage, such as a clock pulse, is applied to the gate, the electric field so produced induces a thin P-type channel across the surface of the N-type region connecting the source and the drain, permitting a current to pass between them. See In re Carlson, 56 CCPA 1309, 412 F.2d 255, 162 USPQ 233 (1969). Fig. 2 is a circuit diagram of a dynamic shift register employing the IGFET device of Fig. 1 **[*568]** as a switch to control a bit of information stored in capacitor C, which may be distributive capacitance of the circuit.

n2 A P-type semiconductor contains more holes, or electron gaps in the lattice of the material, than it does electrons free of covalent bonds in the lattice. An N-type material has an excess of free electrons over holes. These electrons and holes are referred to as "carriers"; "minority carriers," mentioned infra, are electrons in P-type semiconductors and holes in N-type semiconductors. **[**3]**

According to the application,

* * * since the gate G(1) of an insulated gate-type field effect transistor Q(1) as shown in Figure 1 has a high capacitive input impedance, a very small amount of electric charge accumulated on the gate G(1) induces a high voltage and sometimes causes the insulating film (usually silicon dioxide) between the gate G(1) and semiconductor substrate 1 to break down.Therefore, it has been proposed that a protective diode be formed, i.e. a zener diode Rec(1), integrally in the semiconductor body 1 and that the diode be connected in parallel with the gate G(1) as shown in Figure 1. It has been believed that the protective diode could prevent the insulating film from breakdown without interfering with the characteristics of the field effect transistor.

Appellants claim to have discovered that when IGFETs having protective diodes formed in the same substrate, as shown in Fig. 1, are used as switches for storing information or input signals in a memory element having very small capacitance (C on Fig. 2), parasitic transistor action between the protective diode and the drain region may take place when the PN junction J(R) of the protective diode Rec(1) is **[**4]** forward biased n3 by a noise signal, causing the signal stored in the memory element to discharge through the drain region D(1) despite the lack of a pulse applied to the gate electrode. The solution to this problem found by appellants, which they claim as their invention, is a voltage-limiting means auxiliary to the protective diode, which can be a high resistance or another protective diode (hereinafter called "shunt diode"), formed outside the substrate or electrically isolated from other circuit elements on the substrate, connected in parallel with and in the same direction as the protective diode Rec(1).

n3 "Forward bias" is the application of a potential difference to a P-N junction in the direction which aids current flow across the junction.

Claim 1, with reference letters keyed to Fig. 1 and emphasis supplied, is illustrative:

1. In a semiconductor device comprising:

an insulated gate-type field effect component [Q(1)] including a semiconductor substrate [1] of first conductivity type, source [S(1)] and drain [D(1)] regions of second conductivity type opposite to said first conductivity formed in a surface of said semiconductor substrate, and an insulated **[**5]** gate electrode [G (1)] disposed on said surface between said source and drain regions and insulated from said substrate by an insulating film [SiO(2)]; and

a protecting semiconductor diode [Rec(1)] formed integrally in said substrate and connected in parallel between said insulated gate electrode and said semiconductor substrate for protecting the insulating film interposed between said gate electrode and said substrate from breakdown; the improvement comprising

auxiliary means connected with said semiconductor device for preventing minority carriers from said protecting semiconductor diode from reaching said drain region through said semiconductor substrate when noise signals are applied to the protecting diode.

Claim 2 is similar to claim 1 and is cast in the same "Jepson" form. Dependent claims 3-8 depend from claim 2 and recite various added limitations. Claim 33 defines a "memory circuit device" containing appellants' invention. If claim 1 is patentable, so are the other claims.

The Rejection

The examiner cited Bergersen et al. [Bergersen] U.S. patent 3,408,511, issued October 29, 1968 on an application filed May 13, 1966. The Bergersen specification states **[**6]** in part:

This invention relates to an improved insulated-gate field-effect transistor (IGFET) circuit having large bipolarity **[*569]** voltage capabilities. This circuit is operative as an active component of an electronic chopper or an electronic analog switching circuit and is adapted to receive large bipolarity analog input signal voltages.

When an insulated-gate field-effect transistor is used in analog switching or chopper circuits, it must be voltage controlled in such a manner that the P-N junctions between semiconductor substrate and source regions and between semiconductor substrate and drain regions do not become forward biased and enable current to flow from either the substrate region to the source region or from the substrate region to the drain region, respectively. This requirement means that the insulated-gate field-effect transistor can only handle input signals of a limited amplitude if these signals are connected directly in parallel with either of the above defined P-N junctions and between one of the source or drain regions and the substrate region, which is usually at ground potential. If, using the above-described connection, the input signals applied **[**7]** across either of the P-N junctions would be at a voltage level sufficiently high to forward bias these P-N junctions into conduction, then an alternative input signal connection must be resorted to. One such alternative connection involves disconnecting the substrate region from its ground return and from the source of input signals, leaving the substrate region floating. This mode of IGFET operation will prevent the P-N junctions between substrate and source regions and between substrate and drain regions from becoming forward biased, but it will also subject the substrate region to extraneous noise pickup and this is obviously an undesirable compromise for enabling the insulated-gate field-effect transistor to handle large bipolarity signals connected between either source or drain and substrate regions.

* * *

A feature of this invention is the provision of an insulated-gate field-effect transistor circuit including adjacent source, substrate and drain regions with a P-N junction between the substrate and source regions and a P-N junction between the substrate and drain regions. A voltage limiting circuit is connected to the substrate region and includes a diode which is **[**8]** connected between the substrate region and either the source or the drain region. This diode becomes conductive for large amplitude signals of one polarity which are applied to one of the source or drain regions and thereby protects one of the above-identified P-N junctions from becoming forward biased. When large amplitude input signals of an opposite polarity are applied to the same source or drain region, this diode becomes reverse biased and prevents the input signals from reaching the other of the two P-N junctions, and forward biasing this junction.

* * *

The substrate region * * * and the source and drain regions * * * are analogous to two spatially separated diodes connected back to back. Since the source and drain regions * * * are isolated by the substrate region * * * any drain to source current or source to drain current in the absence of a gate voltage is extremely low. The P-N junctions * * * of the so-called back to back diodes defined above must not be allowed to become forward biased for any amount of channel conduction since this would cause extraneous currents to flow to the input and output circuits of a practical chopping or switching device * * *. **[**9]**

It is significant that Bergersen does not explicitly disclose a protective diode formed in the same substrate as the IGFET so protected.

In order to understand one of appellants' arguments, we must look to the PTO position as it developed. In his **[*570]** first rejection of the appealed claims the examiner said:

Applicant's [sic] figures 1 and 2 [reproduced supra] illustrate the prior art. Bergersen et al teach the prevention of a diffused N region in a P substrate from being biased in the forward direction by the input signals through the use of a shunt diode and a resistor. Pursuant to this teaching it is obvious to one of ordinary skill in the art to prevent any of the diode junctions of Applicant's [sic] prior art figures from becoming forward bias [sic] through the use of a shunt diode. No new novel or unexpected result is seen to occur by so doing.

The Examiner's Answer on appeal states that "Applicant's [sic] figure 1 shows the prior art," and concludes:

In the prior art diode protected IGFET the protection diode is usually used to prevent spurious signals, i.e. noise from damaging the date insulator. Noise is usually bipolar. As such it is rather **[**10]** apparent that

the noise signal will forward bias the prior art protection diode. Thus the prior art protection diode is known to operate on bipolar signals, both positive and negative, otherwise only half the protection for the gate insulator would be present. Bergersen et al disclose that noise signals will undesirably forward bias junctions of an IGFET. Forward biased junctions in IGFET'S are undesirable as they create leakage currents between the input and output. The solution to the problem as per Bergersen et al is to prevent the junction from becoming forward biased by shunting the junction with a diode of lower threshold voltage. Pursuant to this teaching it is obvious to one of ordinary skill in the art to add a shunt diode across the protection diode of the prior art that becomes forward biased during half of the protection function. No new, novel, or unexpected results are seen to occur by so doing. Germanium diodes are well known to have a lower threshold voltage than silicon diodes, thus being an obvious design choice to use in the application of the teachings of Bergersen et al.

The board adopted the examiner's reasoning and added some of its own, stating: **[**11]**

We find it logical to apply the teaching of Bergersen et al. to any junction on a single chip. One skilled in the art having studied Bergersen et al. and looking at appellants' Figure 1 would realize and understand that a diode provided purely for gate protection which is integrated into the same chip as the FET might be a source of undesired minority carrier injection from forward biasing in the same way as the source or drain in a field effect transistor as described by Bergersen et al.

* * *

We have no doubt that the examiner is relying on the admitted prior art of Figures 1 and 2 of appellants' drawing. We agree with appellants that the dotted line showing of the transistor action resulting from the forward biasing of the protective diode as depicted in Figure 2 should not be considered as prior art. The dotted line showing clearly represents appellants' contribution and in our opinion the examiner has so construed it.

OPINION

Appellants' brief now questions the PTO's use of Figs. 1 and 2 of their application as "prior art" under 35 USC 103, arguing that there is no statutory basis for considering Figs. 1 and 2 to be "prior art" in the § 103 sense. The oath in the **[**12]** application shows that appellants are citizens and residents of Japan; presumably the invention was made in Japan. Appellants point out that what may have been known to them in Japan would not be prior art by virtue of any portion of 35 USC 102.

We see no reason why appellants' representations in their application should not be accepted at face value as admissions that Figs. 1 and 2 may be **[*571]** considered "prior art" for any purpose, including use as evidence of obviousness under § 103. In re Garfinkel, 58 CCPA 883, 887, 437 F.2d 1000, 1004, 168 USPQ 659, 662 (1971); In re Hellsund, 59 CCPA 1382, 1387, 474 F.2d 1307, 1311, 177 USPQ 170, 173 (1973). n5 By filing an application containing Figs. 1 and 2, labeled prior art, ipsissimis verbis, and statements explanatory thereof n6 appellants have conceded what is to be considered as prior art in determining obviousness of their improvement. That appellants' invention may have been made in Japan is of no consequence in light of their admission.

n5 Although the author of this opinion did not join the opinion of the court in Hellsund, there was no disagreement among the members of the court with the basic proposition that HN1 a statement by an applicant, whether in the application or in other papers submitted during prosecution, that certain matter is "prior art" to him, is an admission that that matter is prior art for all purposes, whether or not a basis in § 102 can be found for its use as prior art. The point of controversy in Hellsund was not whether a binding admission had been made, but what was admitted.The opinion of the court called it an admission of "prior art," but the author of this opinion found it to be an admission merely that the Opel patent contained a disclosure of an invention made prior to Hellsund's invention.

n6 The application contains a section entitled "Description of the Prior Art," which explains Figs. 1 and 2 in detail. We note also that appellants, in an amendment to the application and in their briefs on appeal to the board, repeatedly acknowledged that Figs. 1 and 2 illustrate the prior art. **[**13]**

It is necessary to consider everything appellants have said about what is prior art to determine the exact scope of their admission. The relevant portion of the specification under the heading "Description of the Prior Art" states:

According to investigation, however, it has been revealed that since the PN junction J(R) of the diode Rec(1) is biased in the forward direction by noise pulses e(N), a bipolar transistor is formed [with] the region 2 (as an emitter), the substrate 1 (as a base) and the drain region D(1) of the field effect transistor Q(1) (as a collector) since the junction J(D1) is usually biased in the backward direction. Minority carriers injected into the substrate 1 from the diode region 2 diffuse in the substrate 1 and reach the drain region D(1), as shown by the broken line arrow in Figure 1. [Emphasis added.]

The board in its opinion, supra, conceded that the bipolar transistor action described by appellants in the passage above quoted was not part of the admitted prior art. n7 Therefore, on this record, the admission is only that the structure shown in Figs. 1 and 2 combining an IGFET and its protective diode in a common substrate and the use of that **[**14]** structure in a dynamic shift register circuit were known to the art when appellants invented their improvements.

n7 It is clear from the specification that the dotted line on Fig. 2 referred to by the board represents the same phenomenon as the "broken line arrow" on Fig. 1.

What w said in In re Sponnoble, 56 CCPA 823, 832-33, 405 F.2d 578, 585, 160 USPQ 237, 243 (1969), is relevant here:

It should not be necessary for this court to point out that HN2 a patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the "subject matter as a whole" which should always be considered in determining the obviousness of an invention under 35 USC 103. In re Antonson, 47 CCPA 740, 272 F.2d 948, 124 USPQ 132; In re Linnert, 50 CCPA 753, 309 F.2d 498, 135 USPQ 307. The court must be ever alert not to read obviousness into an invention on the basis of the applicant's own statements; that is, we must view the prior art without reading into that art appellant's teachings. In re Murray, 46 CCPA 905, 268 F.2d 226, 122 USPQ 364; In re Sporck, 49 CCPA 1039, 301 F.2d 686, 133 USPQ 360. **[**15]** The issue, then, is whether the teachings of the prior art would, in and of themselves and without the benefits of appellant's disclosure, make the invention as a whole, **[*572]** obvious. In re Leonor, 55 CCPA 1198, 395 F.2d 801, 158 USPQ 20.

See also In re Conover, 49 CCPA 1205, 304 F.2d 680, 134 USPQ 328 (1962). Appellants' specification identifies the problem discovered by them in part as follows:

The emitter common current amplifier factor $ of this transistor structure [Fig. 1] is in the order of 10(-3) to 10(-4). This factor of the transistor structure is much smaller than those of usual bipolar transistors (in the order of several tens to several hundreds). Therefore, the parasitic bipolar transistor seems to be of negligible value because of the extremely small crurrent amplifier factor.

When an insulated gate-type field effect transistor having a protective diode is used as a control switch for storing an information signal or an input signal in a memory element having very small capacitance, the parasitic bipolar transistor, according to our study, cannot be neglected even if the current amplifier factor [*] is extremely small as aforementioned. * * * **[**16]**

Since the zero voltage level part of the pulse V(CP), however, often includes a noise signal e(N) [Fig. 2] which comprises high frequency components of fairly large amplitude, * * * the diode Rec(1) is biased in the forward polarity by the noise signal e(N). Only in this instant, a parasitic bipolar transistor Q(3) is

constructed, the collector current i(C) flows through the transistor Q(3) and the capacitor C in spite of the OFF-state of the transistor Q(1). Therefore the stored charge in the capacitor C discharges. Especially in such a memory circuit device as that which uses a capacitive memory element of very little capacitance an extremely small amount of collector current i(C) of the parasitic transistor Q(3) causes the [charge] stored in the capacitor C to be reduced considerably since the amount of the stored charge is very small, and it results in misoperation of the memory circuit device.[HN3]

If, as appellants claim, there is no evidence of record that a person of ordinary skill in the art at the time of appellants' invention would have expected the problem in the IGFET to exist at all, it is not proper to conclude that the invention which solves this problem, which **[**17]** is claimed as an improvement of the prior art device, n8 would have been obvious to that hypothetical person of ordinary skill in the art. The significance of evidence that a problem was known in the prior art is, of course, that knowledge of a problem provides a reason or motivation for workers in the art to apply their skill to its solution. Logically, the instant situation is one step removed from the circumstances illustrated by Elbel Process Co. v. Minnesota & Ontario Paper Co., 261 U.S. 45, 67-68 (1923), where the problem of rippling in paper produced on Fourdrinier paper-making machines at high speed was known, but the source of the problem was not.

n8 The matter in claim 1 before the word "improvement" reads on Fig. 1, supra. By using this "Jepson" form, appellants are relying solely on the subject matter following "improvement" to provide patentable distinction over the prior art.

Thus, we must first ask the question: does Bergersen, when considered in conjunction with the prior art structures disclosed in Figs. 1 and 2, suggest the existence of the problem solved by appellants? We think not. While we agree with the PTO that Bergersen supplies the obvious expedient **[**18]** of using voltage-limiting means to prevent the injection of minority carriers (i.e., extraneous currents) from a forward-biased PN junction of the IGFET into the IGFET substrate, we find nothing in Bergersen which, when applied to a structure having a protective diode disposed in a common substrate with an IGFET and not insulated electrically therefrom, is evidence that a person of ordinary skill in the art would have recognized that the misoperation of IGFET memory elements employing such a protective diode was caused by forward biasing of the PN junction, not of the IGFET, but of **[*573]** the protective diode. Bergersen, in fact, is better evidence for the conclusion that a person of ordinary skill in the art would consider that the protective diode Rec(1) of Fig. 1 would prevent injection of minority carriers into the IGFET substrate, not be a cause thereof.

The board attempted to overcome the lack of nexus between Bergersen's teachings and the structure of Fig. 1 by saying that "it [is] logical to apply the teachings of Bergersen et al. to any junction on a single chip." There must, however, be a reason apparent at the time the invention was made to the person of ordinary **[**19]** skill in the art for applying the teaching at hand, or the use of the teaching as evidence of obviousness will entail prohibited hindsight. Graham v. John Deere Co., 383 U.S. 1, 36 (1966). From the portion of Bergersen quoted supra, it appears that the single protective diode of Bergersen would protect one IGFET PN junction from becoming forward biased when signals of a particular polarity are applied to the source or drain region of the IGFET, and would protect the other PN junction when signals of the reverse polarity are applied. While this teaching is available to show that any PN junction may be protected from forward bias by a shunt diode, it does not suggest a problem, or the solution thereto, concerning an IGFET with a protective diode formed in the same substrate in the absence of knowledge that forward bias on the protective diode causes parasitic transistor action or other undesirable phenomena between the PN junction of the protective diode and the source-substrate or substrate-drain PN junction of the IGFET. Parasitic transistor action for the IGFET use contemplated by appellants was a significant source of faulty operation. The board recognized that appellants contributed **[**20]** this knowledge.

The solicitor's argument begs the question:

While it may be true that appellants were the first to recognize and describe the existence of a "parasitic bipolar transistor," that recognition and description, while a professional credit to appellants, is not sufficient to establish the patentability of the claims. After all, what causes the existence of the parasitic bipolar

transistor in appellants' system is the forward biased P-N Junction - the same problem recognized in the Bergersen patent.

It is, of course, not the same problem since Bergersen makes no suggestion that bipolar transistor action might occur when the protective diode and IGFET are formed in a common substrate.

On this record, therefore, we find no evidentiary basis for the finding that a person of ordinary skill in the art would have had reason to apply an additional shunt diode (or other voltage-limiting means) to an IGFET already equipped with a protective diode formed in the same substrate.

The rejection of claims 1-8 and 33 is reversed.

REVERSED